

### **Election/Restriction of Claims**

With respect to a telephone conversation on August 8, 2002 between the Examiner and Kevin L. Daffer, a provisional election was made with traverse to prosecute the semiconductor structure as recited in claims 1-13, 17-21, and 23-25. As such, non-elected claims 14-16, 22, and 26-28 have been canceled. However, Applicants reserve the right to file a divisional application at a later date capturing the subject matter recited in non-elected claims 4-16, 22, and 26-28.

### **Objections to the Drawings**

In the Office Action Summary, the Examiner accepted the drawings as submitted. In the Detailed Action, however, the drawings were objected to under 37 CFR 1.83(a), for failing to show every feature of the invention specified in the claims. As such, the Applicant assumes the acceptance of the drawings in the Office Action Summary is erroneous and, therefore, responds to the drawing objections as set forth in the Detailed Action. In particular, the statement in the Office Action stating, “the ‘first portion’ and ‘second portion’ must be shown or the feature(s) canceled from the claim(s),” (Office Action, page 3), is hereby respectfully traversed.

Claim 1 states, in part: “...a buried layer formed within the substrate below the well region ... and wherein the buried layer includes a first portion underlying the transistor and a second portion spaced apart from and laterally surrounding the first portion.” The Applicant asserts that the “first portion” and “second portion” features, as recited in claims 1, 2, 4, 5, and 23 are shown in the Figures. Fig. 8, for example, illustrates a first portion, such as central portion 86, underlying well region 50 and a second portion, such as annular region 88, spaced apart from and laterally surrounding the first portion. Further support for showing the “first portion” and “second portion” features in Fig. 8 may be found in the Specification, for example, on page 3, lines 29-30, page 4, line 1 and on page 15, lines 3-18. Therefore, the removal of the objection to the drawings is respectfully requested.

### **Section 112 Rejections:**

Claims 1-13 and 23-25 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. A claim is said to be indefinite when it contains words or phrases whose meaning is unclear. If

the scope of a claim would be reasonably ascertainable by those skilled in the art, then the claim is not indefinite. *Ex Parte Porter*, 25 USPQ2d 1144, 1145 (Bd. Pat. App. & Inter. 1992); MPEP 2173.05(e). When the Specification states the meaning that a term in the claim is intended to have, the claim is examined using that meaning, in order to achieve a complete exploration of the applicant's invention and its relation to the prior art. *In re Zletz*, 893 F.2d 319, 13 USPQ2d 1320 (Fed. Cir. 1989); MPEP 2173.05(a). As will be set forth in more detail below, the § 112, second paragraph, rejections of claims 1-13 and 23-25 are respectfully traversed.

The Office Action states, “[i]t is not clear what is meant by the following: a) ‘a second portion spaced apart from and laterally surrounding the first portion’ (See Claim 1); b) ‘first portion’ (See Claims 1 and 4-6); and c) ‘second portion’ (See Claims 1, 2, 4, and 5).” (Office Action, page 3). As noted above, however, the Specification does show support for the “first portion” and “second portion” features, as recited in claims 1-13 and 23-25. For example, the Specification teaches, “[t]he buried layer may be formed in two portions: a central portion underlying the transistor, and a separate portion spaced apart from and laterally surrounding the central portion.” (Specification, page 3, line 29 - page 4, line 1). With respect to Fig. 8, the Specification teaches the buried layer includes central portion 86 and surrounding annular portion 88, which is spaced apart from and laterally surrounding central portion 86. (*see* Specification, page 15, lines 3-5). Furthermore, Fig. 8 illustrates a first portion (i.e., central portion 86) and a second portion (i.e., annular portion 88) spaced apart from and laterally surrounding the first portion. In this manner, a “first portion” and a “second portion spaced apart from and laterally surrounding the first portion” is described in the Specification as components of the “buried layer.” As such, the meaning of the terms “first portion”, “second portion”, and “a second portion spaced apart from and laterally surrounding the first portion” are clear, and the scope of the claim is reasonably ascertainable by those skilled in the art. Therefore, claims 1-13 and 23-25 are definite.

For at least the reasons cited above, claim 1 particularly points out and distinctly claims the subject matter, which the Applicant regards as the invention. Thus, claim 1 and any dependents therefrom are definite. As such, removal of the 35 U.S.C. § 112, second paragraph, rejection of claims 1-13 and 23-25 is respectfully requested.

## **Section 102 Rejections**

Claims 1-3, 6-9, and 11 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4,862,242 to Wildi et al. (hereinafter "Wildi"). As set forth in more detail below, the §102 rejections of claims 1-3, 6-9, and 11 are hereby respectfully traversed.

The standard for "anticipation" is one of fairly strict identity. A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. Of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987), MPEP 2131. Wildi does not teach or suggest all limitations of the currently pending claims, some distinctive limitations of which are set forth in more detail below.

**Wildi does not teach or suggest a first portion of a buried layer underlying a transistor and a second portion of a buried layer spaced apart from and laterally surrounding the first portion.** Independent claim 1 states in part: "a buried layer formed within a substrate below the well region, wherein the buried layer is of opposite conductivity type than the well region, and wherein the buried layer includes a first portion underlying the transistor and a second portion spaced apart from and laterally surrounding the first portion."

Wildi discloses a semiconductor wafer with an electrically isolated semiconductor device. (Wildi, Title). Wildi, however, does not teach or suggest a first portion of a buried layer underlying the transistor and a second portion of a buried layer spaced apart from and laterally surrounding the first portion. Instead, Wildi teaches, "a high voltage tub 114, the upper portion of which comprises N+ high voltage region 116 and the lower portion of which comprises N+ buried layer 118." (Wildi, column 3, lines 5-8). Wildi, however, does not teach or suggest that buried layer 118 is separated into first and second portions, where the second portion is spaced apart from and laterally surrounding the first portion, as illustrated in Fig. 8 of the present invention. Instead, Wildi specifically teaches N+ high voltage region 116 is an upper portion of high voltage tub 114 -- not a second portion of buried layer 118 -- and that N+ high voltage region 116 is arranged above and in contact with buried layer 118, as stated in column 3, lines 25-26 and shown in Fig. 1 of Wildi. Thus, N+ high voltage region 116, as taught by Wilde, is not a second portion of a buried layer spaced apart from and laterally surrounding a first portion of the buried layer, as taught in present claim 1.

In another example, Wildi teaches “N+ high voltage region 116 is laterally spaced by a minimum, predetermined distance X from a P+ ground region 126 that is at a ground 115 potential...” (Wildi, column 3, lines 47-49). Though Wildi teaches P+ ground region 126 is spaced apart from buried layer 118, P+ ground region 126 cannot be the second portion of the buried layer, as recited in the present claims, since P+ ground region 126 and buried layer 118 have opposite conductivity types. Thus, P+ ground region 126, as taught by Wildi, is not a second portion of a buried layer spaced apart from and laterally surrounding a first portion of the buried layer, as taught in present claim 1. Consequently, Wildi does not teach or suggest all limitations of present claim 1.

In addition, Wildi cannot be modified to teach or suggest a first portion of a buried layer underlying a transistor and a second portion of the buried layer spaced apart from and laterally surrounding the first portion, since such a modification would render the invention of Wildi unsatisfactory for its intended purpose. If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984); MPEP 2143.01. For example, the Specification teaches applying a voltage only to the second portion of the buried layer, such that the first portion of the buried layer remains floating. In particular, the Specification states “[d]oped annular structure 52 is connected to outer buried layer portion 88. In this way, inner buried layer portion 86 remains floating no matter what voltage is applied to annular structure 52.” (Specification, page 15, lines 5-7).

Contrary to the teachings of the Specification, however, Wilde teaches it is “desirable to maintain a uniform potential throughout N+ high voltage tub 114” (Wilde, column 4, lines 27-28). In addition, Wilde teaches N+ high voltage tub 114 as including N+ high voltage region 116 and buried layer 118, as stated above and illustrated in Fig. 1. In this manner, if the invention of Wilde were modified to include a buried layer having a first portion and a second portion spaced apart from and laterally surrounding the first portion, the modified invention of Wilde could not maintain a uniform potential throughout N+ high voltage tub 114. If the invention of Wilde were modified to include first and second portions of a buried layer, for example, voltage would be applied only to the second portion of the buried layer and the first portion of the buried layer would remain floating. Thus, modifying the invention of Wilde to include a buried layer having first and second portions, as taught in the present claims, would not maintain a uniform potential throughout the N+ high voltage tub 114, and therefore, would render the invention of Wilde

unsatisfactory for its intended purpose. Consequently, Wildi cannot be modified to teach or suggest all limitations of present claim 1.

For at least the aforementioned reasons, Wildi does not teach or suggest and cannot be modified to teach or suggest all limitations of independent claim 1. Therefore, independent claim 1 as well as claims dependent therefrom, are patentably distinct over Wildi. Accordingly, removal of the §102(b) rejection of claims 1-3, 6-9 and 11 is respectfully requested.

### **Section 103 Rejections**

Claims 4, 5, 10, 17-19, and 23-25 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Wildi. In addition, claims 12, 13, 20, and 21 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Wildi in view of U.S. Patent No. 6,051,868 to Watanabe et al. (hereinafter "Watanabe"). As set forth in more detail below, the rejections of claims 4, 5, 10, 17-19, and 23-25 are hereby respectfully traversed.

To establish a *prima facie* obviousness of a claimed invention, all claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974); MPEP 2143.03. Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed.Cir. 1988); *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992); and, MPEP 2143.01. The cited art does not teach or suggest all limitations of the currently pending claims, some distinctive limitations of which are set forth in more detail below.

**None of the cited art teaches or suggests, or can be combined or modified to teach or suggest, a buried layer of opposite conductivity type than a well region, where the buried layer includes a first portion underlying a transistor and a second portion spaced apart from and laterally surrounding the first portion.** As stated above, independent claim 1 discloses a buried layer of opposite conductivity type than a well region, where the buried layer includes a first portion and a second portion spaced apart from and laterally surrounding the first portion.

As noted in the above § 102 arguments, Wildi does not teach or suggest and cannot be modified to teach or suggest a buried layer having a first portion and a second portion spaced apart from and laterally surrounding the first portion. As such, Wildi cannot be modified to teach or suggest a buried layer of opposite conductivity type than a well region, where the buried layer includes a first portion underlying a transistor and a second portion spaced apart from and laterally surrounding the first portion, as recited in present claim 1.

In addition, Watanabe cannot be combined with Wildi to overcome the deficiencies therein. In particular, Watanabe does not teach or suggest a buried layer of opposite conductivity type than a well region. Instead, and as shown in Fig. 1B, Watanabe specifically teaches a semiconductor device including a transistor (e.g. transistor 108) formed in a well region (e.g., n-type layer 101) and a buried layer (e.g., n-type first buried layer 102), which is formed below the well region and exhibits the same conductivity type as the well region (Watanabe, column 4, lines 14-20). As such, Watanabe does not teach or suggest a buried layer of opposite conductivity type than a well region, as recited in present claim 1. Consequently, Watanabe does not teach or suggest all limitations of present claim 1.

Furthermore, Watanabe cannot be modified to teach or suggest a buried layer of opposite conductivity type than a well region, since Watanabe does not suggest the desirability to make such a modification. The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990); MPEP 2143.01. For example, Watanabe discloses a prior art semiconductor device in which “cross talk is generated between a first n-type buried layer 202 and a second n-type buried layer 203 due to parasitic capacitance between the first n-type buried layer 202 and a p-type semiconductor substrate 200...” (Watanabe, column 1, lines 52-56). In addition, Watanabe discloses another prior art semiconductor device in which “cross talk through the p-type substrate 200 can be reduced, as shown in FIG. 7, by forming an earth-contact layer 724 under n-type buried layer 202 and 203” (Watanabe, column 1, lines 65-67, column 2, line 1). However, Watanabe also discloses that such a “structure for reducing cross talk is not suitable...,” in some cases, since “...the parasitic capacitance between these buried layers 202 and 203 and the p-type high concentration earth-contact layer 724 increases”, thereby increasing cross talk (Watanabe, column 2, lines 18-24). As such, Watanabe describes prior art methods in which cross talk is undesirably generated due to parasitic capacitance between layers of opposite conductivity type. In an effort to overcome the problems of the above-mentioned prior art, Watanabe specifically teaches a semiconductor device including a buried layer (e.g., n-type buried layer

102 of Fig. 1B) of the same conductivity type as a well region (e.g., n-type epitaxial layer 101 of Fig. 1B). Therefore, Watanabe does not suggest the desirability to include a buried layer of opposite conductivity type than a well region, and thus, cannot be modified to include such a buried layer. Consequently, Watanabe cannot be combined with Wilde to teach or suggest all limitations of present claim 1.

**None of the cited art teaches or suggests, or can be combined or modified to teach or suggest metallization adapted to connect a well region to one polarity of a supply voltage, while prohibiting connection of a doped annular region to the other polarity of the supply voltage.** Independent claim 17 states, in part: “[m]etallization adapted to connect the well region to one polarity of a supply voltage for the integrated circuit, while precluding connection of the doped annular region to the other polarity of the supply voltage.”

Wildi does not teach or suggest, nor can Wildi be modified to teach or suggest, the aforementioned limitation of present claim 17. In fact, the Office Action admittedly states “[i]n regards to claim 17, Wildi fails to disclose the following: metallization adapted to connect the well region to one polarity of a supply voltage for the integrated circuit, while precluding connection of the doped annular region to the other polarity of the supply voltage.” (Office Action, page 7). As such, Wildi does not teach or suggest metallization adapted to connect a well region to one polarity of a supply voltage, while prohibiting connection of a doped annular region to the other polarity of the supply voltage, as recited in present claim 17. Therefore, Wildi does not teach or suggest all limitations of present claim 17.

In addition, Watanabe cannot be combined with Wildi to overcome the deficiencies therein. In particular, Watanabe does not teach or suggest metallization adapted to connect a well region to one polarity of a supply voltage, while prohibiting connection of a doped annular region to the other polarity of the supply voltage. Instead, Watanabe teaches that by connecting buried layers associated with different transistors (e.g., buried layers 111 and 112 associated with transistors 108 and 109, respectively) to independent power supplies, via “first and second electrodes 106 and 107, respectively, cross talk through the epitaxial layers and buried layers can be eliminated.” (Watanabe, column 4, lines 46-56, column 5, lines 4-6). As such, Watanabe specifically teaches connecting individual buried layers to different power supplies. Nowhere within Watanabe, however, does it even mention metallization, such as an electrode or interconnect, which is adapted to connect epitaxial layer 101 (e.g., a well region) to a supply voltage, while prohibiting connection of n-type layers 115 (e.g., a doped annular region) to the other polarity of the supply voltage. As such, Watanabe does not suggest the desirability to include metallization adapted to

connect a well region to one polarity of a supply voltage, while prohibiting connection of a doped annular region to the other polarity of the supply voltage. The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990); MPEP 2143.01. Therefore, Watanabe cannot be modified to teach or suggest all limitations of present claim 17. Consequently, Watanabe cannot be combined with Wildi to overcome deficiencies therein.

Furthermore, the statement in the Office Action suggesting, “the limitation of ‘metallization’ makes it a product by process claim” (Office Action, page 7), is hereby respectfully traversed. The Applicant asserts herein the term ‘metallization’ is a structural limitation of the claimed semiconductor device -- not a process. Thus, the term ‘metallization’ in the above limitation does not render claim 17 a product-by-process claim. In particular, the Specification teaches “[m]etallization layer 38, [is] arranged above epitaxial layer 26 and the circuit portions, [and] generally includes conductive contact structures and interconnects interposed with insulation materials.” (Specification, page 7, lines 5-8). In addition, the Specification teaches, “[t]he metallization of the integrated circuit, which includes interconnects 72 and 74 and contact pads 80 and 82, is therefore adapted ... to connect well region 50 and doped annular region 52 to opposite polarities of the supply voltage for the circuit portion.” (Specification, page 13, line 29 – page 14, line 2). As such, the Specification clearly describes the term ‘metallization’ as a structural component of the claimed semiconductor device, and therefore, does not claim a process of making the interconnects and/or contact pads corresponding to the metallization structure. Consequently, the limitation of ‘metallization’ is not a product-by-process claim, thus, claim 17 is patentable.

For at least the reasons set forth above, none of the cited art, either individually or in combination, teaches, suggests, or provides motivation for all limitations of independent claims 1 and 17. Therefore, independent claim 1 and 17, as well as claims dependent therefrom, are patentably distinct over the cited art. Accordingly, Applicants respectfully request removal of the § 103 rejections of claims 4, 5, 10, 12, 13, 17-21, and 23-25.

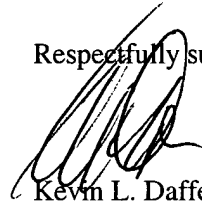


## CONCLUSION

This response constitutes a complete response to all issues raised in the Office Action mailed August 14, 2002. In view of the remarks traversing the rejections, Applicant asserts that pending claims 1-13, 17-21 and 23-25 are in condition for allowance. If the Examiner has any questions, comments, or suggestions, the undersigned attorney earnestly requests a telephone conference.

No fees are required for filing this amendment; however, the Commissioner is authorized to charge any additional fees, which may be required, or credit any overpayment, to Conley, Rose & Tayon, P.C. Deposit Account No. 50-1505/5298-04500.

Respectfully submitted,



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**ATTACHMENT A**  
**“Marked-Up” Amendments**

**IN THE SPECIFICATION**

Please amend pg. 15, line 11 - pg. 16, line 3, as follows:

The buried layer of Fig. 8 may be formed in a similar manner as described above for buried layer 56, but using a different patterned mask layer for the impurity introduction discussed with reference to Fig. 2. For example, rather than forming a single opening in a masking layer (e.g., a photoresist layer) as may be done to form n+ structure 42 of Fig. 2, two openings in a masking layer are formed to introduce impurities for buried layer portions 86 and 88. The spacing needed between two such openings in the masking layer depends on the final separation of the buried layer portions desired, allowing for diffusion during processing. The final desired separation in turn depends on details, such as doping levels, of the particular fabrication process used. In some embodiments, for example, a masking layer spacing of about 2.1 microns may result in a post-processing separation of about 1.2 microns between the buried layer portions. In an embodiment, the separation between the buried layer portions after processing is such that the oppositely-doped region between the portions is “pinched off” during operation by depletion regions at the lower end of the buried layer, while retaining some undepleted material at the upper end of the buried layer. Such an embodiment is illustrated using dashed-line depletion region boundaries 90 in Fig. 8. The buried layer [may] separation may be designed so that the “pinch-off” occurs when outer buried layer portion 88 is connected to VCC (for an n+ buried layer). This “pinch-off” may substantially reduce [substantially] the coupling of noise generated by n-channel transistor 63 to p-type substrate 46. It is noted that no new photolithography masks are required for implementation of the buried layer embodiments described herein (as compared to a conventional fabrication process using buried layers). The structures described herein may instead be implemented by modification of an existing buried layer mask.

**IN THE CLAIMS**

Please cancel claims 14-16, 22, and 26-28.